Amendments to the Specification:

Please replace the paragraph beginning on page 3, line 6 with the following amended paragraph:

However, as shown in FIG. 10, if the time tRC is relatively short with respect to the cycle of the clock signal CLK, it is difficult to externally input the precharge command signal PRC in the DRAM. In FIGs. 9 and 10, WL[0] shows an operation of a selected word line.

Please replace the paragraph beginning on page 6, line 5 with the following amended paragraph:

FIG. 1 schematically illustrates a structure of a DRAM according to the first embodiment. The DRAM comprises an address buffer circuit 11, a command buffer circuit 12, and a memory cell array 13. The address buffer circuit 11 receives an address signal Add, and outputs an internal address signal Addx. The command buffer circuit 12 receives an active command signal ACT, a refresh command signal REF, and write/read command signal W/R from the outside, in accordance with a clock signal CLK. The command buffer circuit 12 generates an internal precharge command signal PRCx and an internal active command signal ACTx, in response to the active command signal ACT. The command buffer circuit 12 also generates an internal refresh command signal REFx and an internal write/read command signal W/Rx, in response to the refresh command signal REF and the write/read command signal W/R, respectively. The memory cell array 13 has a structure in which a plurality of memory cells are arranged in rows and columns. The memory cell array 13 selects one of the memory cells, in response to the precharge command signal PRC and each of the internal command signals fed from the command buffer circuit 12 and the address signal from the address buffer circuit 11, and performs an operation, such as data writing or reading, with respect to the selected cell.

Please replace the paragraph beginning on page 8, line 20, with the following amended paragraph:

FIG. 3B schematically illustrates the structures of the row control section 13a and the row decoder 13b. The row decoder 13b includes ~~is provided with~~ drivers 13e and 13f, ~~for example,~~ which are connected in series. The driver 13e receives an ouput signal of a decoding circuit (not shown), and the driver 13f drives ~~drive~~ the word lines in response to an output signal of [[a]] the

decoding circuit ~~(not shown)~~.

Please replace the paragraph beginning on page 10, line 19, with the following amended paragraph:

FIG. 5 illustrates an operation in reading of data. The horizontal axis shows time in nanoseconds (t(ns)). When precharge is performed in response to the precharge command signal PRCx, the bit lines BL and /BL are precharged with a voltage of VDD/2, for example. In this state, if the word line WL is selected, the word-line monitor signal /WLUP changes to low level, and the potentials of the bit lines BL and /BL change according to data stored in the memory cell. The sense amplifier 13c senses and amplifies the potentials of the bit lines BL and /BL. Thereafter, precharge is performed by a precharge command signal PRCx of the next cycle. Further, when the internal active command signal ACTx changes to low level, the word line WL is rendered unselected. Precharge of the bit lines and decoding of the row address are performed in a period Tpd in which the precharge command signal PRCx and the internal active command signal ACTx are at low level.

Please replace the paragraph beginning on page 13, line 22, with the following amended paragraph:

An active command signal ACT outputted from the command buffer circuit 12 is supplied to, for example, a counter 15a, together with a clock signal CLK. The counter 15a counts a selected time of a word line, and counts the clock signal CLK in response to the active command signal ACT. Specifically, the counter 15a is a so-called preset counter. A value corresponding to the maximum selected time of a word line is preset in the counter 15a, and the counter 15a generates an output signal TIMEUP when a counted value reaches the preset value. The output signal TIMEUP is supplied to one input end of a flip-flop circuit 15b. The other input end of the flip-flop circuit 15b is supplied with the active command signal ACT. The flip-flop circuit 15b is set by the output signal TIMEUP of the counter 15a, and reset by the active command signal ACT. The set output signal of the flip-flop circuit 15b is supplied as a precharge request signal PRCREQ to a latch circuit 15c, together with the clock signal CLK. An output signal of the latch circuit 15c is supplied to a logic circuit 15d, together with the clock

signal CLK. An output signal of the logic circuit 15d is supplied to an OR circuit 15e, together with an output signal of a logic circuit 12b. An output signal of the OR circuit 15e is outputted as an internal precharge command signal PRCx, through an inverter circuit 15f.